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Abstract of the Disclosure

A method for use by a host microprocessor which translates sequences of instructions from a target instruction set for a target processor to sequences of instructions for the host microprocessor including the steps of beginning execution of a speculative sequence of target instructions by committing state of the target processor and storing memory stores previously generated by execution at a point in the execution of instructions at which state of the target processor is known, executing the speculative sequence of host instructions until another point in the execution of target instructions at which state of the target processor is known, rolling back to last committed state of the target processor and discarding the memory stores generated by the speculative sequence of host instructions if execution fails, and beginning execution of a next sequence of target instructions if execution succeeds.